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(54)【発明の名称】　マスク形成方法

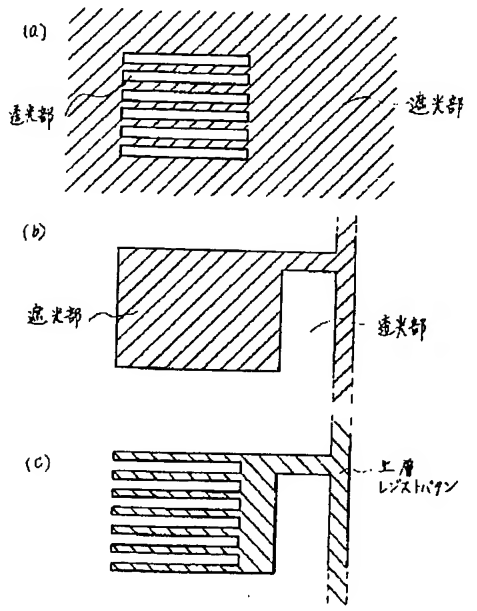
(57)【要約】

【目的】　デバイスのパタン形成に際して上記デバイスの極微細パタン領域の露光に対しては位相シフトマスクを、また、その他のパタン領域の露光には通常の透過型マスクを用いた縮小投影露光で適用することにより達成される。

【構成】　一枚又は異なるマスク上に位相シフトマスク領域と透過型マスク領域を有し試料上の同一位置に重ね露光させる。これを用いれば、上記極微細パタン領域と回路パタン領域を上記試料上に同時に露光することができる。

【効果】　極微細パタンを有するデバイスのパタン形成において、簡便かつスループットの大きい、経済性に優れた微細素子の形成方法を提供することにある。

図１



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【特許請求の範囲】

【請求項1】所望のパターンを与えるマスクパターンの露光領域を、第1の露光領域と第2の露光領域に分解する工程、

第1の露光領域を含む第1のマスクと第2の露光領域を含む第2のマスクを形成する工程、を含み上記第1のマスクと上記第2のマスクの少なくともどちらか一方は、隣接する光透過部を通過する光の位相を反転させる位相シフトパターンを含む位相シフトマスクであることを特徴とするマスク形成方法。

【請求項2】上記所望のパターンが、第1のマスクにより実質的に形成される非露光領域、及び第2のマスクにより実質的に形成される非露光領域の和領域に一致する、ことを特徴とする請求項1記載のマスク形成方法。

【発明の詳細な説明】

【0001】

【産業上の利用分野】本発明は、寸法0.2μm～0.1μm以下の極微細パタンを有する半導体または超電導素子の製造厘方法に係り、特にこれらの素子に好適なパタン形成方法に関する。

【0002】

【従来の技術】パーミアブル・ベース・トランジスタ（以下ＰＢＴ）または各種量子井戸アレイデバイス、超マトリクス固体発振子、ラテラル超格子ＦＥＴ、共鳴トンネリング効果デバイス等の量子効果デバイスの作製においては、素子内に極めて微細な格子状，縞状，又は点状パタンの集合等を作製する必要がある。これらのデバイスの多くは量子効果をねらっており、そのパタン周期は、0.1μm程度からそれ以下であることが望まれる。

【0003】従来、これらの素子はＥＢ（電子ビーム）又はＦＩＢ（集束イオンビーム）の直接描画により作製されてきた。ＥＢを用いた量子効果デバイスの作製に関しては、例えば、ソリッド・ステート・テクノロジー，１９８５年，１０月号，第１２５頁から第１２９頁（Solid State Technology/Octover,１９８５，ｐｐ１２５－１２９）に論じられている。

【0004】一方、縮小投影光法による光リソグラフィの限界解像度は，露光波長に比例し、縮小レンズの開口数に反比例する。現在エキシマレーザ（KrFレーザ，波長２４８ｎｍ）と開口数0.4～0.5の縮小レンズを用いて0.3μm程度が達成されている。又、開口数0.5の反射光学系とＡｒＦエキシマレーザ（波長１９３ｎｍ）を用いて0.13μmを解像した例がある。（ジャーナル オブ バキューム サイエンス アンド テクノロジー Ｂ５（１），１９８７年，１／２月号，第３８９頁から第３９０頁（J. Vac. Sci. Technol. B5(1), Jan/Feb １９８７，ｐｐ３８９－３９０））。

【0005】ところで、縮小投影露光法における解像限界を向上する方法に位相シフト法がある。位相シフト法

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によれば、その解像限界は通常の透過型マスクによる露光法を用いた場合の２倍程度向上する。従って、これによれば0.15μmから0.1μm以下の微細パタンを形成することが可能である。この位相シフト法は、特別な露光装置を必要とせず、通常の縮小投影露光装置において、従来の透過型マスク（レチクル）を位相シフトマスク（レチクル）に変更するだけで行なうことができる。位相シフト法に関しては例えば、アイ・イー・イー・イー；トランザクション オン エレクトロン デバイシズ，イーデー３１，ナンバー６（１９８４）第７５３頁から第７６３頁（IEEE, Trans. Electron Devices, Vol, ＤＥ－３１，No.６（１９８４），ｐｐ７５３－７６３）に論じられている。

【0006】また、光を用いて縮小投影露光法の解像限界以下のパタンを形成する別の方法に、ホログラフィ法があるが、このホログラフィ法は特殊な露光装置を必要とし、しかもパタンはウエハの全面に形成され、そのパタンを、基板上に既に存在するパタンに対して位置合わせすることができない。この様なホログラフィ法については、例えば昭和５９年秋季、第４５回応用物理学会学術講演会、講演予講集第２４２頁に論じられている。

【0007】

【発明が解決しようとする課題】上記のＥＢ，ＦＩＢによる極微細パタンの描画作製には、多大の時間を要し、経済性が悪いという問題点があった。

【0008】一方、縮小投影露光法の限界解像度ではＰＢＴ、量子効果デバイス等に必要な0.1μm以下のパタンを形成することは非常に困難である。

【0009】位相シフト法を用いればこれを達成することが可能である。しかしながら、位相シフト法の弱点として、実際のＬＳＩパタンの様な複雑なマスクパタンに対応するのが困難なことがあげられる。位相シフト法は、単純なラインアンドスペースパタン（以下Ｌ／Ｓ）、格子パタン、点状パタン等の作製に関して、非常に有効な技術である。

【0010】本発明の目的は、極微細パタンを有するデバイスのパタン形成において、上記問題点を解決し、簡便かつスループットの大きい、経済性に優れた微細素子の形成方法を提供することにある。

【0011】

【課題を解決するための手段】上記目的は、上記デバイスのパタン形成に際して上記デバイスの極微細パタン領域（例えばＰＢＴのグリッド部分）の露光に対しては位相シフトマスクを、また、その他のパタン領域の露光には通常の透過型マスクを用いた縮小投影露光で適用することにより達成される。

【0012】

【作用】本発明が対象とするデバイスのパタンは、単純な繰り返し構造を有する極微細パタンの密集領域と、制御電極や配線等の比較的複雑な構造を有する回路領域に

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2分される。これらの2つの領域はデバイス製造プロセスにおける同一層内に混在する場合もあり、又、別々の層として存在する場合もある。

【0013】前者の極微細パタン領域は単純なL／S、点状パタン集合、格子状パタンで、その寸法は0.1μm程度、もしくはそれ以下であり、その形状も比較的単純である。この領域内のパタン形成は位相シフトマスク（レチクル）を用いた縮小投影露光法により可能となる。

【0014】一方、後者の回路領域におけるパタンの寸法は前者より大きく、従来の透過型マスク（レチクル）を用いた縮小投影露光法により形成するのが適している。

【0015】上記2つの領域を別々に露光する際には、両者の位置合せを行なう必要がある。通常合せ精度は少なくとも最小寸法の半分以下に抑えなければならない。従って、0.1μmのパタンに対しては0.05μm以下の合せ精度が必要となるが、現在この様な精度をもつ露光装置はない。しかし、本発明における2つの領域間の合せ精度は、通常の露光装置の保障する程度の値で十分である。何故ならば、本発明の対象となるデバイスにおける極微細パタンは全体として機能し、従って極微細パタン領域と回路パタン領域の相対位置は所定の範囲内に収める必要があるものの、極微細パタンの一つひとつの位置精度はそれほど厳密さを要求されない。

【0016】前記二つの領域が同一層内に混在する場合には、一枚のマスク上に位相シフトマスク領域と透過型マスク領域を混在させることもできる。これを用いれば、上記極微細パタン領域と回路パタン領域を1枚のマスクで同時に露光することができる。但し、この場合、二つの領域の接続部において解像不良の生じる恐れがある。即ち、位相の異なる2つの透光部が接する場合、干渉によりここで光強度が低下する。この様なパタンの配置は避けなければならない。

【0017】本発明によれば、パタンの露光は縮小投影露光法により行なわれるので、電子ビーム，集束イオンビームの直接描画による方法に比してはるかに短時間でこれを完了することができる。

【0018】又、本発明によれば、特殊な露光装置を必要とせず、露光フィールド内の所望の位置に極微細パタンを形成することができるため、ホログラフィ法より有利である。

【0019】

【実施例】

（実施例1）以下、本発明を用いたＰＢＴの製造方法の実施例を示す。

【0020】まず、キャリア収集電極層に形成したＧａＡｓ基板上にさらにW薄膜を形成し、その上に、下層有機膜／中間層無機膜／上層レジスト膜の3層構造からなる、いわゆる3層レジストを形成した。上層レジストとしてはＰＭＭＡ（ポリメチルメタクリシート）を用いた。次に、図1（a）に示した様なＰＢＴの制御電極領域の極微細L／Sだけを有する位相シフトレチクルを用いて露光を行なった。位相シフトレチクルの微細L／Sにおける隣り合う透光部は、照明光の位相を互いに180°反転させる様配置されている。次に、図1（b）に示した様な制御電極周辺回路パタンを有する透過型レチクルに交換し、露光を行なった。

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【0021】上記2つの領域に対する露光は、基板を露光装置の基板ステージ上に固定したままレチクルのみを変更して、連続的に行なわれる。各々の露光において位置合わせ操作を行なうことはいうまでもない。又は、上記2つの領域に対する露光の順番は特に規定しない。使用した露光装置の光源はＫｒＦエキシマレーザ，光学系の開口数は0.6である。1露光フィールドにおいて上記2枚のレチクル各々の露光に要する時間は約5秒であった。一方、電子線描画装置を用いて同一パタンの露光を行なったところ、これに要する時間は約600秒であった。

【0022】次に、上記上層レドストの現像を行ない、図1（c）に示した様な上層レジストパタンを得た。これを反応性イオンエッチングにより順次前記中間層、下層へ転写した。その結果、上記下層有機膜において前記極微細制御電極パタン領域におけるアスペクト比の高い矩形断面形状を有するL／Sパタンと、前記周辺回路パタンの両方が得られた。

【0023】こうして形成した下層有機層パタンをマスクとしてW膜のドライエッチングを行ない、制御電極パタンを形成した後、その上にＧａＡｓを成長させ制御電極を埋め込み、ひき続きキャリア注入電極、配線等を形成してＰＢＴを作製した。上記制御電極パタン以外の露光は全て透過型マスクを用いた。作製したＰＢＴの電気特性を評価した結果、所期の性能が得られた。

【0024】なお、図1は説明のための模式的な平面であり、必ずしも実際のトランジスタのレイアウトを表示したものではない。また、デバイス構造，基板材料，制御電極材料，レジスト材料およびプロセス，露光装置等に関しても、本実施例に示したのに限らず使用することができる。

【0025】本実施例の露光過程は、ＰＢＴに限らず単純な極微細L／Sパタンと周辺回路の混在する他のデバイス例えばラテカル1次元超格子ＦＥＴ等に対しても適用できる。

【0026】（実施例2）ＰＢＴにおいては、極微細パタン領域と回路パタン領域が同一層（制御電極層）内に混在するので、上記各領域に対応して位相シフトマスク領域と透過型マスク領域の混在するレチクルによりパタンを形成できる。このためのマスクを図2に示す。前記実施例1においては、制御電極形状は図1（c）に示したごとくくし型であった。しかし本方法においては位相

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シフトマスク領域と透過マスク領域を完全に分離するために、透過型マスク領域内の完全な遮光部中に位相シフト型マスク領域（図2中点線内）を配置した。

【0027】（実施例3）本発明を用いて超マトリクス固体発振素子の製造方法に関する一実施例を示す。　GaAs基板上にポジ型レジストPMMAを塗布し、図3に示す様なドット状の透光部の集合をもつ位相シフトマスクで露光を行なった。その後現像して図3の透光部の各々に対応したレジスト開口部を得た。位相シフトマスクの各透光部は照明光の位相を上下左右の両方向に交互に180°反転させる様に（市松模様状に）配置されている。なお、位相シフトマスクには、図3に示したドット状透光部の各々の周囲に位相反転用のより微細な透光部パタンを設けてもよい。

【0028】次に、メタライゼーションを行ない、レジスト上およびレジスト開口部の基板上に金属を蒸着した後、レジストを除去してリフトオフ法により基板上にメタルドット行列を形した。ひき続き電極等を形成して超マトリクス固体発振素子を製造した。

【0029】ここでは固体発振素子の製造への実施例を示したが、本実施例のレジストパタン形成工程をGaAs基板上のメタライゼーションに代えて、他の様々なプロセスと組み合せることにより、種々のデバイスへの応用が可能である。例えばGaAs基板上にGaAlAs薄膜を成長させた後、ネガ型レジストと本実施例による位相シフトマスクを用いてパタン形成を行なうと、図3のドット状透光部の各々に対応してレジストパタンが残る。これをマスクにGaAlAsの異方性エッチングを行ない、適当な後処理を行なうことにより量子井戸行列を形成することができる。同様に、ラテラルFET超格子、共鳴トンネリング効果トランジスタ等への応用が可能である。

【0030】（実施例4）本発明を用いた超マトリクス固体発振素子の製造方法に関する別の実施例を示す。

【0031】前記実施例3におけるポジ型レジストをネガ型レジストに置き換え、さらに、露光プロセスを以下

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の様に変更した。まず図4に示す様なマスクA，マスクB，マスクCを用意した。マスクA及びBはL／S位相シフトマスクで、各々におけるL／Sは互いに直交しているか、もしくは基準方向に対して異なる角度をもっている。A，B及びCの3枚のマスクを用いて、同一レジスト膜上に重ね露光することにより、実施例3と同様のレジストパタンを得た。即ちドット行列はマスクA及びBにおけるL／Sの重なり部分に形成され、マスクCはドット行列領域の範囲を規定する。本実施例によれば、実施例3と比べてドット行列の周期をより小さくすることが可能で、しかもレジストの平面的形状を角ばらせることができる。

【0032】本実施例のパタン形式工程が、実施例3と同様様々なデバイスに応用可能であることはいうまでもない。

【0033】

【発明の効果】以上本発明による半導体又は超電導体装置の製造方法によれば、量子効果素子等における0.1μm程度からそれ以下の寸法のパタンから成る極微細パタン領域を含む回路パタンの形成過程において、上記極微細パタン領域の露光を位相シフト法を用いた縮小投影露光法により、それ以外の回路パタンを通常の露光法により各々独立に行なうことにより、上記パタン形成に要する時間を著しく短縮するとともに、装置コストを低減することができる。

【0034】これにより、上記半導体・超電導体素子の量産における経済性を向上させることができる。また、上記素子が集積化された場合において、これらの効果は一層顕著となる。

【図面の簡単な説明】

【図1】本発明の実施例におけるマスクパタンの平面図。

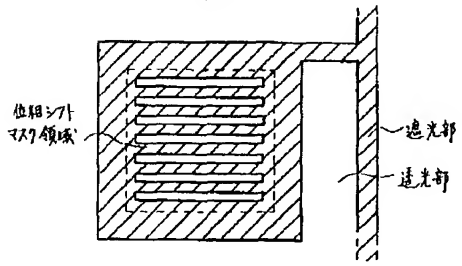
【図2】透過型マスク領域内の遮光領域中に位相シフトマスク領域を配置したことを示す図。

【図3】ドット状透光部の集合を示す図。

【図4】マスクパタンの平面図。

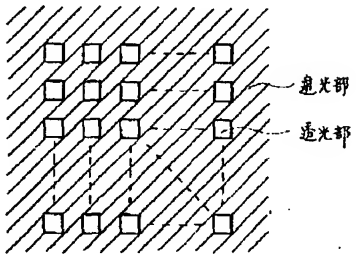
【図2】

図2



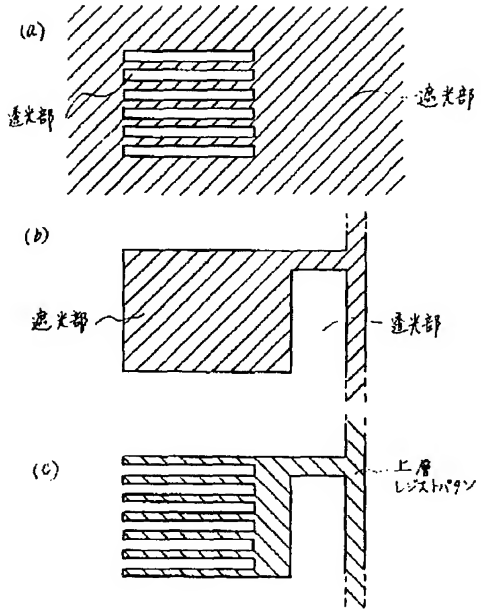
【図3】

図3



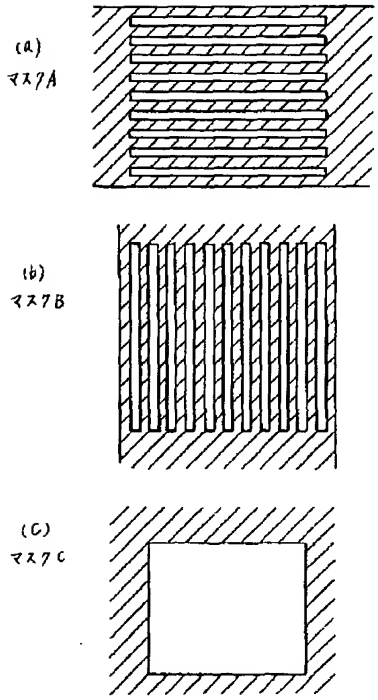
【図１】

図１



【図４】

図４



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Continued on last page

(54) **[Title of the Invention]** Mask Formation Method

(57) **[Abstract]**

[Object]

At the time of formation of a pattern for a device, [the object is] achieved by the application of photoreduction-projection exposure using a phase-shift mask for the exposure of ultrafine-pattern regions of the aforementioned device, and a normal transmission-type mask for the exposure of other pattern regions.

[Composition]

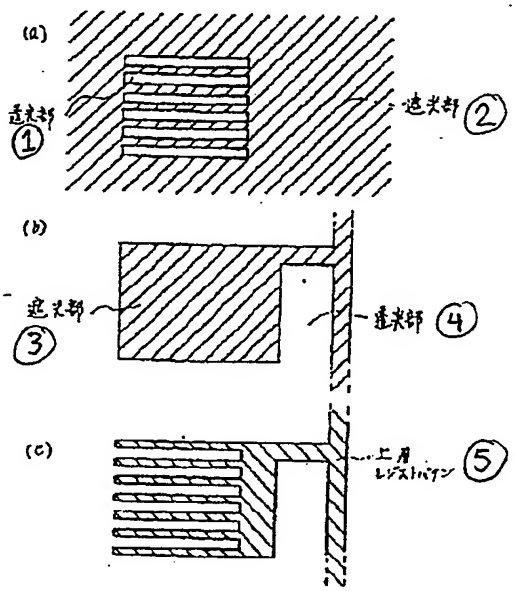
One or [several] different masks have a phase-shift mask region and a transmission-type mask region which are exposed when overlaid at the same position upon a sample. By using this, the aforementioned ultrafine-pattern regions can be exposed simultaneously with the circuit pattern region upon the aforementioned sample.

[Meritorious Effects]

In the process of pattern formation for a device having an ultrafine pattern, this invention provides a method of formation of fine devices which is simple, has high throughput and is economical.

Fig. 1

図1



[Key]

1. Translucent area
2. Opaque area
3. Opaque area
4. Translucent area
5. Top-layer resist pattern

[Claims]

[Claim 1]

A mask formation process comprising the steps of:

a step wherein the exposed region of the mask pattern to be given the desired pattern is broken down into a first exposed region and a second exposed region; and

a step wherein a first mask containing the first exposed region and a second mask containing the second exposed region are formed; and

characterized in that at least one of said first mask and said second mask is a phase-shift mask containing a phase-shift pattern that reverses the phase of light transmitted through the adjoining light-transmitting area.

[Claim 2]

The mask formation process according to claim 1, characterized in that the aforementioned desired pattern matches the sum region of the non-exposed region essentially formed on the first mask and the non-exposed region essentially formed on the second mask.

[Detailed Description of the Invention]

[0001]

[Field of the Invention]

This invention relates to a method of manufacturing* semiconductor or superconductor devices having an ultrafine pattern with dimensions of 0.2 μm-0.1 μm or less, and particularly to a pattern formation method suited to these devices.

[0002]

[Prior Art Statement]

In the manufacture of permeable-base transistors (PBT) or various quantum well array devices, super-matrix solid-state oscillators, lateral super-lattice FETs, resonant tunneling effect devices or other quantum-effect devices, it is necessary to fabricate within the device extremely fine lattice-shaped, stripe-shaped or sets of point-shaped patterns. Many of these devices aim at achieving quantum effects, so their pattern period is preferably roughly 0.1 μm or below.

[0003]

Conventionally, these devices have been fabricated by means of direct electron beam (EB) or focused ion beam (FIB) lithography. The fabrication of quantum-effect devices using EB is discussed in Solid State Technology, October, 1985, pp. 125-129 (Solid State Technology/Octover [sic], 1985, pp. 125-129), for example.

[0004]

On the other hand, the limit resolution of optical lithography by means of photoreduction-projection optical methods is proportional to the exposure wavelength and inversely proportional to the numerical aperture of the photoreduction lens. Currently, roughly 0.3 μm has been

*Translator's note: The character *rin* (an ancient Japanese unit of money, weight or length) appears between the words "method" and "manufacturing." It appears to be a typographical mistake.

achieved using an excimer laser (KrF laser, wavelength of 248 nm) and a photoreduction lens with a numerical aperture of 0.4-0.5. In addition, there is an example of resolving 0.13 μm using a reflecting optical system with a numerical aperture of 0.5 and an ArF excimer laser (wavelength of 193 nm) (Journal of Vacuum Science and Technology B5(1), January/February 1987, pp. 389-390 (J. Vac. Sci. Technol. B5(1), Jan/Feb 1987, pp. 389-390)).

[0005]

However, the phase-shift method is a method of increasing the limit resolution of photoreduction-projection exposure methods. The phase-shift method increases the limit resolution to roughly twice that of the case of using exposure methods based on ordinary transmission-type masks. Therefore, this means that it is possible to form fine patterns with dimensions of 0.15 μm to 0.1 μm or less. This phase-shift method does not require special exposure apparatus, but rather it can be performed by simply replacing the conventional transmission-type mask (reticle) with a phase-shift mask (reticle). The phase-shift method is discussed in IEEE; Transactions on Electron Devices, ED-31, No. 6 (1984), pp. 753-763 (IEEE, Trans. Electron Devices, Vol. DE-31, No. 6 (1984), pp. 753-763)

[0006]

In addition, another method of forming patterns at resolutions below the limit resolution of light-based photoreduction-projection exposure methods is the holography method, but this holography method requires special exposure apparatus and moreover, the patterns are formed over the entire surface of the wafer, so the pattern cannot be aligned to patterns already existing on the substrate. This holography method is discussed in the Preprints of the 45th Meeting of the Japan Society of Applied Physics, Fall 1984, p. 242.

[0007]

[Problems Which the Invention is Intended to Solve]

The aforementioned fabrication of ultrafine patterns by EB or FIB lithography has drawbacks in that it requires large amounts of time and is uneconomical.

[0008]

On the other hand, with the limit resolution of photoreduction-projection exposure methods, it is extremely difficult to form the patterns with dimensions below 0.1 μm required for PBTs, quantum-effect devices and the like.

[0009]

This can be achieved by using the phase-shift method. However, the drawback of the phase-shift method lies in that it is difficult to adapt to complex mask patterns such as those of actual LSI devices. The phase-shift method is an extremely effective technology for the fabrication of simple line-and-space patterns (L/S), lattice patterns, point patterns and the like.

[0010]

The object of the present invention is to solve the aforementioned problems in the pattern formation for devices having an ultrafine pattern, and to provide a method of formation of fine devices which is simple, has high throughput and is economical.

[0011]

[Means of Solving the Problems]

At the time of formation of a pattern for the aforementioned device, the aforementioned object is achieved by the application of photoreduction-projection exposure using a phase-shift mask for the exposure of ultrafine-pattern regions of the aforementioned device, and a normal transmission-type mask for the exposure of other pattern regions.

[0012]

[Function of the Invention]

The patterns for devices to which the present invention applies are divided into a dense region with an ultrafine pattern having simple repetitive structures and a circuit region which has control electrodes, wiring and other relatively complex structures. These two regions can coexist within the same layer in a device fabrication process or they may be present as separate layers.

[0013]

The former ultrafine pattern region may be an L/S, point-shaped pattern set, or lattice-shaped pattern, and its dimensions may be roughly 0.1 μm or below, but its shape is relatively simple. Pattern formation within this region is possible by means of photoreduction-projection exposure methods using a phase-shift mask (reticle).

[0014]

On the other hand, the dimensions of the pattern in the latter circuit region are larger than those of the former, and are suitable to formation by means of photoreduction-projection exposure methods using a conventional transmission-type mask (reticle).

[0015]

At the time of separately exposing the aforementioned two regions, it is necessary to perform the alignment of the two. The alignment precision must normally be kept to at least below half of the minimum feature size. Therefore, an alignment precision of 0.05 μm or less is required for a 0.1 μm pattern, but there is currently no exposure apparatus available that has such precision. However, as the alignment precision between the two regions in the present invention, a value on the level guaranteed by ordinary exposure apparatus is adequate. The reason why is that the ultrafine patterns in the devices to which the present invention applies function as an overall pattern, and so while the positions of the ultrafine pattern region and the circuit pattern region relative to each other must be kept within a stipulated range, not so much strictness is required for the positional precision of each individual ultrafine pattern.

[0016]

In the case wherein the aforementioned two regions coexist within the same layer, it is possible for the phase-shift mask region and the transmission-type mask region to coexist in a single mask. By using this, it is possible to expose both the aforementioned ultrafine pattern region and circuit pattern region simultaneously with a single mask. However, in this case, there is a risk of resolution defects occurring in the portions where the two regions connect. To wit, in the case of contact between two translucent areas having different phases, the light intensity is decreased due to interference. Such pattern layouts must be avoided.

[0017]

By means of the present invention, pattern exposure is performed by means of photoreduction-projection exposure methods, so it can be completed in much shorter time than methods based on direct electron beam or focused ion beam lithography.

[0018]

In addition, by means of the present invention, no special exposure apparatus is necessary and an ultrafine pattern can be formed at any position desired within the exposure field, so it is more advantageous than holography methods.

[0019]

[Working Examples]

(Working Example 1)

Here follows an explanation of one working example of a PBT manufacturing method using the present invention.

[0020]

First, a GaAs substrate is formed as a carrier collection electrode layer and thereupon is formed a W thin film, and thereupon is formed a so-called 3-layer resist having a 3-layer structure consisting of a bottom-layer organic film/intermediate-layer inorganic film/top-layer resist film. PMMA (poly(methyl methacrylate)) is used as the top-layer resist. Next, a phase-shift reticle having only an ultrafine L/S in the control electrode region of a PBT as shown in Fig. 1(a) is used to perform exposure. The adjacent translucent areas in the fine L/S of the phase-shift reticle are laid out such that the phases of illuminating light are inverted by 180° with respect to each other. Next, the reticle is exchanged for a transmission-type reticle that has a control electrode peripheral circuit pattern such as that shown in Fig. 1(b), and exposure is performed.

[0021]

The exposure of the aforementioned two regions is performed consecutively after changing the reticle only with the substrate kept fixed in the substrate stage. Naturally the alignment operations are performed for each exposure. In addition, the order of exposure of the aforementioned two regions is not stipulated. The light source for the exposure apparatus used was a KrF excimer laser, and the numerical aperture of the optical system was 0.6. The time required for the exposure of each of the aforementioned two reticles in one exposure field was approximately 5 seconds. On the other hand, when exposure of the same pattern was performed using an electron beam lithography apparatus, the time required was approximately 600 seconds.

[0022]

Next, development of the aforementioned top-layer resist was performed to obtain a top-layer resist pattern such as that shown in Fig. 1(c). Reactive ion etching was used to transfer this pattern sequentially to the aforementioned intermediate layer and bottom layer. As a result, in the aforementioned lower-layer organic film was obtained both an L/S pattern with a rectangular cross section having a high aspect ratio in said ultrafine control electrode pattern region and said peripheral circuit pattern.

[0023]

The bottom-layer organic-layer pattern thus formed was used as a mask to perform dry etching of the W film, and after forming a control electrode pattern, GaAs was grown thereupon

to embed the control electrode, and then the carrier injection electrodes, wiring and the like were formed to fabricate a PBT. Transmission-type masks were used for all exposure except for that for the aforementioned control electrode pattern.

[0024]

Note that Fig. 1 is a schematic plan diagram used for explanation; it does not necessarily show the layout of an actual transistor. In addition, the device structure, substrate material, control electrode material, resist material and the process, exposure apparatus and the like are in no way limited to those given in this working example, but others may be used.

[0025]

The exposure process of this working example is applicable not only to a PBT but rather it is also applicable to other devices wherein simple ultrafine L/S patterns coexist with peripheral circuits, for example, lateral one-dimensional super-lattice FETs and the like.

[0026]

(Working Example 2)

In a PBT, the ultrafine pattern region coexists with the circuit pattern region within the same layer (the control electrode layer), so the pattern can be formed by means of a reticle wherein the phase-shift mask region and the transmission-type mask region corresponding to the aforementioned regions coexist. A mask for this purpose is shown in Fig. 2. In the aforementioned Working Example 1, the control electrode was shaped like a comb as shown in Fig. 1(c). However, in this method, in order for the phase-shift mask region and the transmission mask to be completely separate, the phase-shift mask region (indicated by dashed lines in Fig. 2) is laid out completely inside an opaque area within the transmission-type mask region.

[0027]

(Working Example 3)

Here follows an explanation of one working example of an super-matrix solid-state oscillator manufacturing method using the present invention. A GaAs substrate is coated with the positive resist PMMA and exposure is performed using a phase-shift mask having a set of dot-shaped translucent areas as shown in Fig. 3. Thereafter, it was developed to obtain resist holes corresponding to each of the translucent areas of Fig. 3. The translucent areas in the phase-shift mask are laid out (in a checkered pattern) such that the phases of illuminating light are alternately inverted by 180° with respect to the adjacent areas in the up/down/left/right directions. Note that

a finer translucent area pattern used for phase reversal may be provided in the periphery of each of the individual dot-shaped translucent areas.

[0028]

Next, metallization is performed, where metal is vapor-deposited upon the resist and upon the substrate in the openings in the resist, and then the resist is removed by the lift-off method to form a matrix of metal dots upon the substrate. Thereafter, electrodes and the like are formed to fabricate a super-matrix solid-state oscillator.

[0029]

Here, we presented a working example of the manufacture of a solid-state oscillator, but by combining the resist pattern formation process of this working example with various other processes instead of metallization upon a GaAs substrate, it can be adapted to various types of devices. For example, after forming a GaAlAs thin film upon a GaAs substrate, by using a negative resist and the phase-shift mask according to this working example to perform pattern formation, a resist pattern corresponding to each of the dot-shaped translucent areas of Fig. 3 remains. By using this mask to perform anisotropic etching of GaAlAs and performing appropriate post-treatment, it is possible to form a quantum well array. In the same manner, this working example is adaptable to lateral super-lattice FETs, resonant tunneling effect transistors and the like.

[0030]

(Working Example 4)

Here follows an explanation of another working example of an super-matrix solid-state oscillator manufacturing method using the present invention.

[0031]

The positive resist in the aforementioned Working Example 3 is replaced with a negative resist and moreover the exposure process is changed as follows. First, a mask A, mask B and mask C as shown in Fig. 4 are prepared. Masks A and B are L/S phase-shift masks wherein the L/S patterns may be perpendicular to each other, or lie at different angles with respect to a reference direction. By using the three masks A, B and C to perform superimposed exposure upon the same resist film, the same resist pattern as in Working Example 3 is obtained. To wit, the dot array is formed by the portions where the L/S patterns overlap in masks A and B, while mask C defines the range of the dot array region. By means of this working example, it is possible to

make the pitch of the dot matrix smaller than that in the case of Working Example 3, and moreover it is possible to vary the angles in the planar shape of the resist.

[0032]

As in the case of Working Example 3, naturally the pattern formation step of this working example can be adapted to various devices.

[0033]

[Meritorious Effects of the Invention]

With the method of manufacturing semiconductor or superconductor devices according to the present invention, in the process of forming circuit patterns in quantum effect devices or the like that have dimensions of roughly 0.1 μm or less, by independently performing the exposure of the aforementioned ultrafine pattern region by a photoreduction-projection exposure method using the phase-shift method, and performing the exposure of other circuit patterns by ordinary exposure methods, it is possible to shorten markedly the time required for the aforementioned pattern formation and reduce the apparatus cost.

[0034]

Thereby, it is possible to make the mass production of the aforementioned semiconductor or superconductor devices more economical. In addition, these effects become even more marked when the aforementioned devices are integrated.

[Brief Explanation of the Drawings]

Fig. 1 is a plan view of mask pattern in a working example of the present invention.

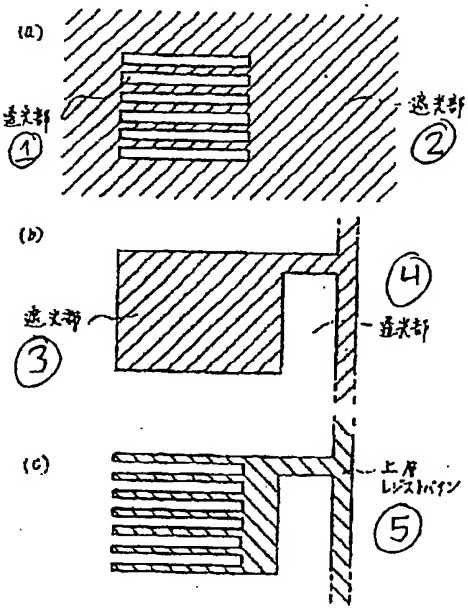
Fig. 2 is a diagram showing the layout of the phase-shift mask region inside the opaque region within the transmission-type mask region.

Fig. 3 is a diagram showing a set of dot-shaped translucent areas.

Fig. 4 is a plan view of a mask pattern.

Fig. 1

図 1

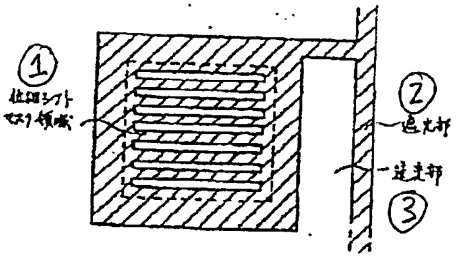


[Key]

1. Translucent area
2. Opaque area
3. Opaque area
4. Translucent area
5. Top-layer resist pattern

Fig. 2

図 2

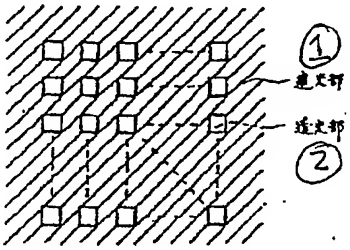


[Key]

1. Phase-shift mask region
2. Opaque area
3. Translucent area

Fig. 3

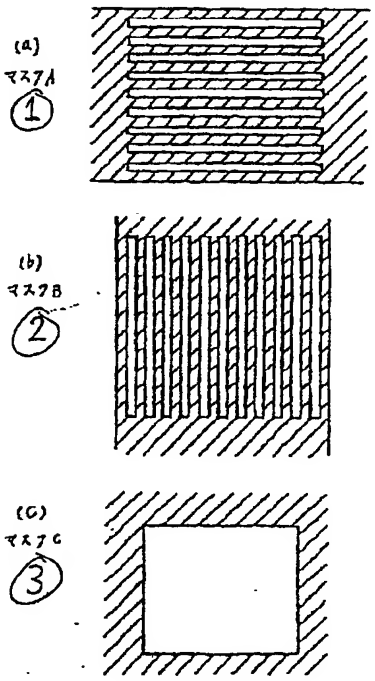
図3



[Key]
1. Opaque area
2. Translucent area

Fig. 4

図4



[Key]
1. Mask A
2. Mask B
3. Mask C

Continuation of Front Page

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Filing Date: May 11. 1988
Assignee: Hitachi Ltd.

Specification

[Title of the Invention]
Method for forming mask

[Claim]
1. A method for forming a mask, comprising;
a step for dividing an exposure area of a mask pattern providing a desirable pattern into a first exposure area and a second exposure area,
a step for forming a first mask including said first exposure area and a second mask including said second exposure area, wherein at least either of said first mask and said second mask is a phase shift mask including a phase shift pattern to invert the phase of the light which passes through adjacent permeable portions.
2. A method for forming a mask as defined in claim 1, wherein said desirable pattern corresponds to an area which is formed by adding a non-exposure area formed substantially by said first mask and a non-exposure area formed substantially by said second mask.

[Detail Description of the Invention]
(Field for Industrial Application)

The present invention relates to a method for producing a semiconductor or superconducting element having a microscopic pattern of 0.1 μm to 0.2 or less in size, in particular to a method for forming a pattern suitable for such an element.

(Prior Art)

In productions of permeable base transistors (hereinafter referred as to PBT) or various quantum well array devices, super matrix solid transmitters, lateral super grid FETs, resonance tunnel effect devices, it is required to create a group of microscopic grid, stripe or dot pattern in an element. Most of these devices aim at taking advantage of the quantum effect and so their pattern period is desirable to be about 0.1 μm or less.

Heretofore, these elements have been produced by means of the direct depiction using EB (Electron Beam) or FIB (Focusing Ion Beam). With regard to the production of quantum effect devices using EB, it is, for example, discussed in "Solid State Technology"/ October, 1985, P125-129.

On the other hand, critical resolution of optical lithography in a reduction projection method is in direct proportion to exposure wavelength and in inverse proportion to numerical aperture of reduction lens. The critical resolution of about 0.3 μm has currently been achieved by using the excimer laser (KrF leaser, wavelength: 248nm) and a reduction lens having the numerical aperture of 0.4 to 0.5. In one example, it has also been reported to resolve o.13 μm by using a catoptic system having the numerical aperture of 0.5 and ArF excimer laser (wavelength: 193 nm) ("Journal of Vacuum Science and Technology" B5(1), Jan/Feb 1987, P389-390).

The phase shift method is one of technique for improving the critical resolution in the reduction projection exposure method. The phase shift method can improve

twice the critical resolution comparing with the exposure method using regular permeable masks. Thus this method enables to form a microscopic pattern of 0.1 μm to 0.15 μm or less. No special exposure equipment is required for this phase shift method. That is, a regular reduction projection exposure equipment can be modified only by change a regular permeable mask (Recherche) to a phase shift mask (Recherche). The phase shift method is discussed in IEEE, "Transaction on Electron Device", Vol. 1, DE-31, No.6 (1984), P753-763.

The holography method is one of different optical methods for forming patterns of certain critical resolution not more than that in the reduction projection exposure method. This holography method requires a particular exposure equipment. Besides the resulting pattern is formed on whole area of a wafer and such a pattern cannot be positioned with respect to the pattern which has previously been formed on a substrate. Such a holography method is, for example, discussed in The 45th Autumn Meeting, 1984, Draft, The Japan Society of Applied Physics, 1997, P242.

[Problem to be solved by the Invention]

When the depiction of microscopic pattern is created by the aforementioned EB or FIB, there is caused problems such as plenty of required time and economical inefficiency.

It is also very difficult to form the pattern of 0.1 μm or less which is necessary for PBTs, quantum effect devices and the like by the reduction projection exposure method due to its insufficient critical resolution.

Such an objective can be achieved by using the phase shift method. However as a weak side of the phase shift method, it is point out that this method cannot be adapted for complicate mask pattern such as actual LSI patters. The phase shift

method has been effective technology only for simply pattern such as line and space pattern (thereinafter referred as L/S), stripe pattern and dot pattern.

It is an object of the present invention to solve the abovementioned problem and provide a simple method for forming microscopic elements, which has high throughput and excellent economical efficiency.

[means for solve the problem]

The abovementioned object is achieved by a reduction projection exposure method in which the phase shift mask is applied to expose a microscopic pattern area, such as grid portion of the PBT, and the regular permeable mask is also applied to expose the other pattern area, in pattern forming process of the aforementioned device.

[Function]

A pattern of devices subject to the present invention is divided into a dense area of microscopic pattern having simply repeated structure and a circuit area having relatively complicated structure such as control electrodes and wirings. These two areas can be mixed in the same layer and otherwise separately in different layers.

The former pattern area is a simple L/S, a group of dot patterns and stripe pattern, It has a size of about 0.1μm or less and relatively simple shape. The reduction projection exposure method using the phase shift mask (Recherche) makes it possible to form the pattern of this area.

The pattern size of the latter circuit area is lager than the former area so that the reduction projection exposure method using the conventional permeable mask (Recherche) may be suitable for forming the latter pattern.

When the aforementioned two areas is separately exposed, it is required to position each other. An accuracy of the positioning must be controlled within at least half of minimum size of the patter. Therefore the pattern of 0.1 μm requires a positioning accuracy of 0.05 μm or less, but there is no exposure apparatus having such an accuracy. However a positioning accuracy for the two areas of the present invention is satisfied with a value as much as that which can be assured by the regular exposure apparatus. Because the microscopic pattern of the device subject to the present invention functions as a whole. Thus while a relative position of the microscopic pattern area and the circuit pattern area is required to control in a predetermined range, each microscopic pattern does not require very strict positioning accuracy.

When the aforementioned two areas is mixed in the same layer, a phase shift mask area and a permeable mask area may be mixed on one mask. With using this mask, the microscopic pattern area and the circuit pattern area can simultaneously be exposed by one mask. However in this case, at a connecting portion on the two areas, some defect of resolution possibly occur. That is, when two light transmission portions having respective different phases are closely situated each other, light intensity would be reduced due to mutual interference. Therefore these arrangement must be avoided.

According to the present invention, since the exposure of the pattern is performed by the reduction projection exposure method, this processing time can be reduced comparing with the method of the direct depiction using electron beam or focusing Ion beam.

Further according to the present invention, since the microscopic pattern can be formed at any desirable position in a exposure field without any specific exposure apparatus, this method is more advantageous than the holography method.

[Embodiment]

(Embodiment 1)

An embodiment of a method for producing the PBT applying the present invention is described hereinafter.

First, a GaAs substrate is formed on a carrier collection electrode layer and a W film is further formed on the GaAs substrate. Then three layers structure, i.e. three layers resist, which is composed of a lower layer organic film, intermediate layer inorganic film and upper layer resist, is formed on the GaAs substrate. A PMMA (polymethyl methacryl sheet) is used as the upper layer resist. Then, the exposure operation is performed by using a phase shift Recherche which has only microscopic L/S for a control electrode area of the PBT as shown in Fig.1(a). In the microscopic L/S of the phase shift Recherche, adjacent light transmission portions are arranged so as to make the phase of irradiation light invert 180 degree each other. Then after changing to a permeable Recherche having a control electrode peripheral circuit pattern as shown in Fig.1(b), the exposure operation is performed.

The exposure operation to the abovementioned two areas is continuously performed with maintaining the substrate fixed on a substrate stage of a exposure apparatus and changing only the Recherches. It goes without saying that an positioning operation is performed in each exposure operation. a sequence of exposure operations for the two areas is particularly defined. The light source of the exposure apparatus used is a KrF excimer laser and its numerical aperture is 0.6. In one exposure field, each exposing time for exposing with each of the two Recherches is about 5 second. On the other hand, a exposure operation is performed by using an electron beam depiction apparatus. As a result, about 600 second is required for this operation.

Then a development operation of the upper layer resist is performed to obtain a resulting upper resist layer as shown in Fig.1(c). This pattern is sequentially transcribed to the intermediate layer and then lower layer by the reactive ion etching process. As a result, in the lower layer organic film, both of a L/S pattern having a high aspect ratio and a rectangular cross sectional shape for the microscopic control electrode pattern area and the peripheral circuit pattern can be obtained.

The W film is processed with dry etching by using this resulting lower organic layer pattern as a mask to form a control electrode pattern. Then on the resulting W film, GaAs is grown, a control electrode is filled in and then a carrier filling electrode, wiring and the like are formed, so that a PBT is produced. All exposure operations are performed by using the permeable mask except for the control electrode pattern. The produced PBT is evaluated in electrical characteristics. As a result, it is confirmed that the desired performance could be obtained.

Since Fig.1 is explanatory typical plan view, actual layout of a transistor is not exactly illustrated. device structures, substrate materials, control electrode materials, resist materials, processes, exposure apparatuses and the like are not limited to specific example described in the present embodiment.

The exposure process of the present embodiment can be applied not only to the PBT but also to other devices, such as lateral one-dimensional super grid FET, in which a simple microscopic L/S pattern and a peripheral circuit are mixed.

(Embodiment 2)

In the PBT, since a microscopic pattern area and a peripheral circuit area are mixed in the same layer (control electrode layer), these patterns can be formed by

a Recherche in which a phase shift mask area and a permeable mask area respectively arranged corresponding to each pattern areas are mixed. Such a mask is shown in Fig.2. In the embodiment 1 described above, the control electrode has a com shape as shown in Fig.1 c). However, in this method, the phase shift mask area (surrounded area by the broken line in Fig.2) is disposed in a portion, where light is wholly blocked, within the permeable mask area so as to completely separate the phase shift mask area and a permeable mask area.

(Embodiment 3)

One embodiment related to a method for producing a super matrix solid oscillation element by using the present invention. A positive type resist PMMA is applied on the GaAs substrate and then a exposure operation is performed by using a phase shift mask having a group of dot permeable portions as shown in Fig.3. Then resist openings corresponding to each permeable portion of Fig.3 can be obtained. Each permeable portion of the phase shift mask is arranged to make the phase of irradiation light invert 180 degree alternately in both of vertical and longitudinal directions (checkered pattern). in the phase shift mask, a permeable portion pattern which is smaller than each of the dot permeable portion may be provided around each periphery of the dot permeable potions shown in Fig.3 in order to invert the phase of irradiation light.

Through the metallization process, metallic material is deposited on the resist and the substrate of the resist openings. Then the deposited metal is removed and metal dot matrix is formed by the lift-off method, followed by forming electrodes and the like, and finally a super matrix solid oscillation element is produced.

While here an embodiment for producing a solid oscillation element is described, the resist pattern forming process of the present embodiment can be mixed various processes as a substitute for the metallization on the substrate, so that

this method can be applied to various devices. For example, after the GaAlAs film is grown on the GaAs substrate, patters are formed by using a negative type resist and the phase shift mask according to the present embodiment, thereby a resist pattern is remained corresponding to each the dot permeable portion of Fig.3. Then the GaAlAs film is processed by the anisotropy etching with using this pattern as a mask. Then after suitable after treatments, a quantum well matrix can be formed. This method can also be applied to leteral FET super grid, resonance tunneling effect transistors and the like.

(Embodiment 4)

Another embodiment related to a method for producing a super matrix solid oscillator element using the present invention.

A negative type resist is substituted for the positive type resist in the embodiment 3 described above, and the exposure process is changed as follows. First, a mask A, mask b and mask C as shown in Fig.4 are prepared. The mask A and B are L/S phase shift masks in which each L/S intersects at right angles each other or has different angles with respect to the reference direction. With using three masks A, B and C, exposure operations are performed with lapping over the exposure on the same substrate, resulting in a resist pattern as same as that of the embodiment 3. Thus a dot matrix is formed on a portion where the L/S of the mask A and B are overlapped, and the mask C defines the dot matrix area. According to the present embodiment, the period of the dot matrix can make smaller comparing with the embodiment 3, and the two-dimensional shape of the resist can be angulated.

It goes without saying that the pattern forming process of the present embodiment can be applied to various devices as well as the embodiment 3.

[Effect of the Invention]

As above, according to the method for producing a semiconductor or superconductor, in a process for forming a circuit pattern which includes a microscopic pattern area composed of a patter of about 0.1 μm or less in size in a quantum effect element and the like, a exposure operation for the microscopic pattern area is performed by the reduction projection exposure method using the phase shift method, and the regular exposure method is separately performed for other circuit patter, which enables the required pattern forming time and the apparatus cost to be reduced.

Thus in mass production of the semiconductor or superconducting element, its economical efficiency can be improved. Further if the element is integrated, this effect would come to front.

[Brief Description of the Drawings]

Fig.1 is a plan view showing a mask pattern according to an embodiment of the present invention.

Fig.2 shows a state in which a phase shift mask area is disposed in a light blocked area of the permeable mask area.

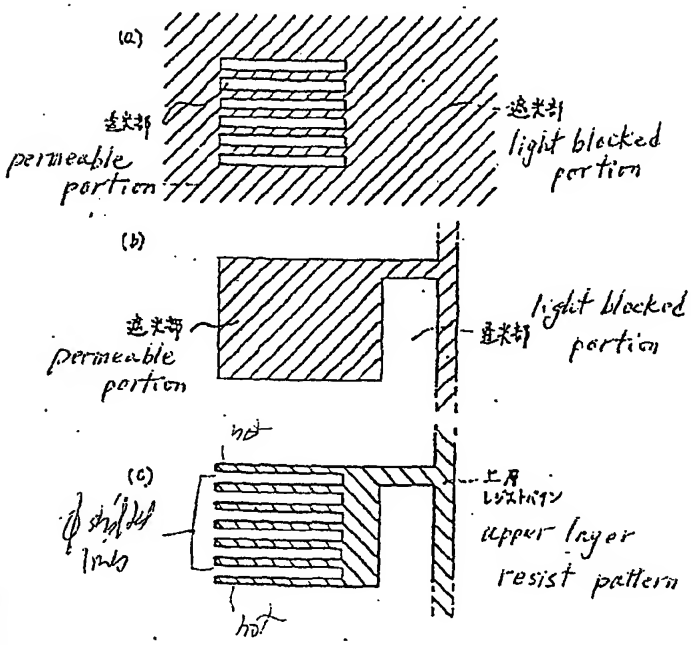
Fig.3 shows a group of dot permeable portions.

Fig.4 is a plan view showing a mask pattern.

【図1】

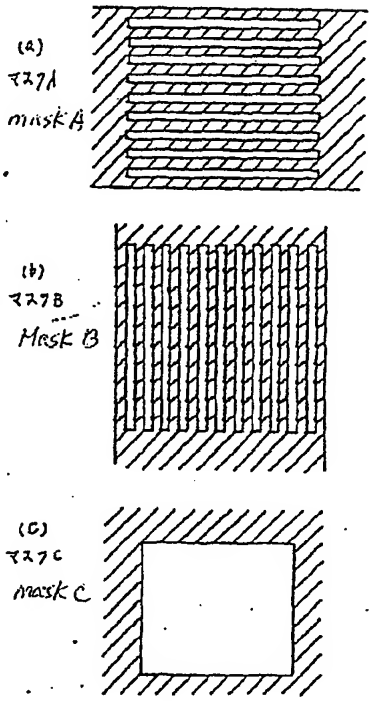
Fig. 1

図1



【図4】

図4



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シフトマスク領域と透過マスク領域を完全に分離するために、透過型マスク領域内の完全な遮光部中に位相シフト型マスク領域（図2中点線内）を配置した。

【0027】（実施例3）本発明を用いて超マトリクス固体発振素子の製造方法に関する一実施例を示す。GaAs基板上にポジ型レジストPMMAを塗布し、図3に示す様なドット状の透光部の集合をもつ位相シフトマスクで露光を行なった。その後現像して図3の透光部の各々に対応したレジスト開口部を得た。位相シフトマスクの各透光部は照明光の位相を上下左右の両方向に交互に180°反転させる様に（市松模様状に）配置されている。なお、位相シフトマスクには、図3に示したドット状透光部の各々の周囲に位相反転用のより微細な透光部パタンを設けてもよい。

【0028】次に、メタライゼーションを行ない、レジスト上およびレジスト開口部の基板上に金属を蒸着した後、レジストを除去してリフトオフ法により基板上にメタルドット行列を形した。ひき続き電極等を形成して超マトリクス固体発振素子を製造した。

【0029】ここでは固体発振素子の製造への実施例を示したが、本実施例のレジストパタン形成工程をGaAs基板上のメタライゼーションに代えて、他の様々なプロセスと組み合せることにより、種々のデバイスへの応用が可能である。例えばGaAs基板上にGaAlAs薄膜を成長させた後、ネガ型レジストと本実施例による位相シフトマスクを用いてパタン形成を行なうと、図3のドット状透光部の各々に対応してレジストパタンが残る。これをマスクにGaAlAsの異方性エッチングを行ない、適当な後処理を行なうことにより量子井戸行列を形成することができる。同様に、ラテラルFET超格子、共鳴トンネリング効果トランジスタ等への応用が可能である。

【0030】（実施例4）本発明を用いた超マトリクス固体発振素子の製造方法に関する別の実施例を示す。

【0031】前記実施例3におけるポジ型レジストをネガ型レジストに置き換え、さらに、露光プロセスを以下の様に変更した。まず図4に示す様なマスクA，マスクB，マスクCを用意した。マスクA及びBはL／S位相シフトマスクで、各々におけるL／Sは互いに直交しているか、もしくは基準方向に対して異なる角度をもっている。A，B及びCの3枚のマスクを用いて、同一レジスト膜上に重ね露光することにより、実施例3と同様のレジストパタンを得た。即ちドット行列はマスクA及びBにおけるL／Sの重なり部分に形成され、マスクCはドット行列領域の範囲を規定する。本実施例によれば、実施例3と比べてドット行列の周期をより小さくすることが可能で、しかもレジストの平面的形状を角ばらせることができる。

【0032】本実施例のパタン形式工程が、実施例3と同様様々なデバイスに応用可能であることはいうまでもない。

【0033】

【発明の効果】以上本発明による半導体又は超電導体装置の製造方法によれば、量子効果素子等における0.1μm程度からそれ以下の寸法のパタンから成る極微細パタン領域を含む回路パタンの形成過程において、上記極微細パタン領域の露光を位相シフト法を用いた縮小投影露光法により、それ以外の回路パタンを通常の露光法により各々独立に行なうことにより、上記パタン形成に要する時間を著しく短縮するとともに、装置コストを低減することができる。

【0034】これにより、上記半導体・超電導体素子の量産における経済性を向上させることができる。また、上記素子が集積化された場合において、これらの効果は一層顕著となる。

【図面の簡単な説明】

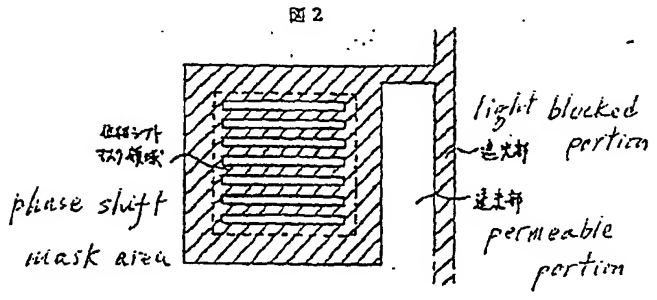
【図1】本発明の実施例におけるマスクパタンの平面図。

【図2】透過型マスク領域内の遮光領域中に位相シフトマスク領域を配置したことを示す図。

【図3】ドット状透光部の集合を示す図。

【図4】マスクパタンの平面図。

【図2】 Fig. 2



【図3】 Fig. 3